* **Register Description**

|  |  |  |
| --- | --- | --- |
| Register Name | Offset Address | Description |
| Control signals | 0x00 | Control signals Definition  bit 0 - ap\_start (Read/Write/COH)  Set 1 to start Axis DMA function  bit 1 - ap\_done (Read/COR)  bit 2 - ap\_idle (Read)  bit 3 - ap\_ready (Read/COR) |
| s2m Buffer transfer done status register | 0x10 | bit 0 – s2m buffer transfer done status (Read)  Set this register to 1 if stream data has written to memory and data length is equal to Buffer Length(640\*480/4 DW) |
| s2m Buffer transfer done status clear register | 0x20 | bit 0 – clear s2m buffer transfer done status (Read/Write)  Set 1 to clear s2m buffer done status/s2m error status and reset internal state, then set 0 if finish to clear buffer done status  Note: Before set this register to 1 to clear s2m buffer transfer done status/s2m error status, Clear status control register must set to 1. After buffer transfer done status is clear, this register needs to be cleared for next operation. |
| s2m Buffer Length | 0x28 | Set s2m buffer length, must set to 640\*480/4. |
| s2m Clear Status Control register | 0x30 | bit 0 –Enable to clear s2m buffer transfer done status (Read/Write) |
| s2m Buffer Lower base address register | 0x38 | bit 31~0 – The memory base address [31:0] of s2m buffer (Read/Write) |
| s2m Buffer Upper base address register | 0x3C | bit 31~0 – The memory base address [63:32] of s2m buffer (Read/Write) |
| s2m err status register | 0x44 | bit 0 – s2m err status when sof(start of frame) signal or eol(end of line) signal of side band of user project is incorrect (Read) |
| Image width | 0x54 | bit 31~0 – Image\_width[31:0] (Read/Write)  Note: The value of this register is DW unit, so the value should be real width divided by 4. This value must be 160, due to Image is 640(width)\*480(height) |
| m2s Buffer Lower base address register | 0x5C | bit 31~0 – The memory base address [31:0] of m2s buffer (Read/Write) |
| m2s Buffer Upper base address register | 0x60 | bit 31~0 – The memory base address [63:32] of m2s buffer (Read/Write) |
| m2s Buffer transfer done status register | 0x68 | bit 0 – m2s buffer transfer done status (Read)  Set this register to 1 if data has fetched from memory and data length is equal to Buffer Length(640\*480/4 DW) |
| m2s Buffer transfer done status clear register | 0x78 | bit 0 – clear m2s buffer transfer done status (Read/Write)  Set 1 to clear m2s buffer done status/s2m error status and reset internal state, then set 0 if finish to clear buffer done status  Note: Before set this register to 1 to clear m2s buffer transfer done status/ m2s error status, Clear status control register must set to 1. After buffer transfer done status is clear, this register needs to be cleared for next operation. |
| m2s Buffer Length | 0x80 | Set m2s buffer length, must set to 640\*480/4. |
| m2s Clear Status Control register | 0x88 | bit 0 –Enable to clear m2s buffer transfer done status (Read/Write) |

* **Porting Guide**

1. Setup process
   1. Set Rx20 to 0x00, exit clear s2m status operation
   2. Set Rx30 to 0x00, disable to clear s2m status operation
2. Set Rx78 to 0x00, exit clear m2s status operation
3. Set Rx88 to 0x00, disable to clear m2s status operation
4. Set Rx28 to (640\*480/4), Set s2m buffer length
5. Set Rx38, Rx3C for the memory base address of s2m buffer
6. Set Rx54 to (640/4), Set Image width(Unit is DW)
7. Set Rx5C, Rx60 for the memory base address of m2s buffer
8. Set Rx60 to (640\*480/4), Set m2s buffer length
9. Set Rx00[0] to 1, set ap\_start register to start the trigger operation
10. Data process
    1. Wait Rx10[0] == 1, indicate the received data fills full the s2m buffer for image conversion completion.
    2. Read all data from buffer
11. Status clear process
    1. Set Rx20[0] to 1, clear s2m Buffer transfer done status clear register and reset internal state
    2. Set Rx30[0] to 1, Enable to clear s2m buffer transfer done status
    3. Set Rx78[0] to 1, clear m2s Buffer transfer done status clear register and reset internal state
    4. Set Rx88[0] to 1, Enable to clear m2s buffer transfer done status
    5. Set Rx00[0] to 1, set ap\_start register to start the trigger operation
    6. Wait (Rx10[0] == 0, Rx68[0] == 0 and Rx44[0] == 0), confirm s2m/m2s/s2m\_err status is cleared
    7. Set Rx20 to 0x00, exit clear s2m status operation
    8. Set Rx30 to 0x00, disable to clear s2m status operation
12. Set Rx78 to 0x00, exit clear m2s status operation
13. Set Rx88 to 0x00, disable to clear m2s status operation